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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
ISAAC, STANETTA D

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/710,001	MO ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed 6/11/04. Currently, claims 1-22 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 6/11/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 20 recites the limitation "said field apertures" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5, 8, 9, 19 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato et al., US Patent 6,798,038.

Sato discloses the semiconductor method as claimed. See figures 1A-12H, and corresponding text, where Sato teaches, pertaining to claim 1, a method of forming a set of insulator plugs in an isolation trench in a semiconductor substrate having a device layer comprising the steps of: depositing a pad insulator layer **3** having a pad thickness over said device layer surface (figure 2A; col. col. 4, lines 9-13); etching a set of apertures **5** through said pad insulator and said device layer to an isolation depth (figure 2D; col. 4, lines 20-24); depositing an isolation insulator layer **7** in said apertures to a depth sufficient to fill said apertures above said device layer by a first margin and having a sidewall thickness on aperture walls (figure 2E; col. 4, lines 25-41); etching said isolation insulator layer such that said sidewall thickness of said isolation insulator on said aperture walls is removed and remaining isolation plugs of said isolation insulator layer fill said apertures with an isolation plug surface above said device layer surface by a second margin (figure 2F; col. 4, lines 42-62); and etching said pad insulator layer with an etchant that does not attack said isolation insulator layer, whereby said

pad insulator is removed and said isolation plugs fill said apertures without CMP (figure 2J; col. 5, lines 9-13).

Sato teaches, pertaining to claim 3, in which said wafer is a bulk silicon wafer in which said device layer is formed in said silicon wafer (figure 2K; col. 5, lines 32-45).

Sato teaches, pertaining to claim 4, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount (figure 2F; col. 4, lines 42-61).

Sato teaches, pertaining to claim 5, in which said first margin is greater than said sidewall threshold amount (figure 2F; col. 4, lines 42-61).

Sato teaches, pertaining to claim 8, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount (figure 2F; col. 4, lines 42-61).

Sato teaches, pertaining to claim 9, in which said first margin is greater than said sidewall threshold amount (figure 2F; col. 4, lines 42-61).

Sato teaches, pertaining to claim 19, a method for forming a set of isolation plugs in an isolation trench in a semiconductor substrate having a device layer comprising the steps of: depositing a pad insulator layer **2/3/60** having a pad thickness (figure 12A; col. 18, lines 3-8); etching a set of apertures through said device layer to an isolation depth (figures 12B and 12C; col. 18, lines 9-26); depositing an insulator layer **7** in said apertures to a depth sufficient to fill said apertures above said device layer by a first margin and having a sidewall thickness on aperture walls (figure 12D; col. 18, lines 27-36); etching said insulator layer such that said sidewall thickness of said insulator on said aperture walls is removed and remaining isolation plugs of said insulator layer fill said apertures substantially coplanar with said device layer (figure 12E; col. 18, lines 37-44); forming a set of apertures in areas of pad insulator disposed

between isolation apertures separated by an minimum active area distance (figure 12E; col. 18, lines 37-44); and etching said pad insulator layer with an etchant that does not attack said insulator layer , whereby said pad insulator is removed and said isolation plugs fill said aperture without CMP (12H; col. 18, lines 52-55).

Sato teaches, pertaining to claim 22, in which said step of etching said insulator layer such that said sidewall thickness of said insulator on said aperture walls is removed and remaining isolation plugs of said insulator layer fill said apertures substantially coplanar with said device layer is performed after said step of forming a set of apertures in area of pad insulator disposed between isolation apertures separated by a minimum active area distance (figure 12H; col. 18, lines 52-55).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al., US Patent 6,798,038 in view of *Stanley Wolf, Silicon Processing For The VLSI Era, 1986, Lattice Press, Vol. II, pages 66-67.*

Sato discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 3-5, 8, 9, 19 and 22 under 35 U.S.C. 102(e). In addition, Sato shows, pertaining to claim 6, in which said pad thickness is less than

a sidewall threshold amount (figure 2F; col. 4, lines 42-61). Also, Sato shows, pertaining to claim 7, in which said first margin is greater than said sidewall threshold amount (figure 2F; col. 4, lines 42-61).

However, Sato fails to show, pertaining to claim 2, in which said wafer is an SOI wafer in which said device layer is formed above a buried insulator layer.

Wolf teaches, on pages 66-67, conventionally known advantages to the use of a silicon on insulator (SOI) substrate.

It would have been obvious to one of ordinary skill in the art to substitute, in which said wafer is an SOI wafer in which said device layer is formed above a buried insulator layer, in the method of Sato, pertaining to claim 2, according to the conventional teachings of Wolf, with the motivation that by using a SOI wafer for a semiconductor device would result in , a reduction in capacitive coupling, an increase in the number of manufactured devices due to a reduction in chip size, and an increase in the circuit speed. Therefore, a semiconductor device formed on an SOI wafer would be prove to be a much more efficient semiconductor device.

Claims 10-18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al., US Patent 6,798,038 in view of Chung US Patent 6,653,201.

Sato discloses the semiconductor substantially as claimed. See figures 1A-12H, and corresponding text where Sato shows, pertaining to claim 10, a method of forming a set of insulator plugs in an isolation trench in a semiconductor substrate having a device layer comprising the steps of: depositing a pad insulator layer **3** having a pad thickness over said device layer surface (figure 2A; col. col. 4, lines 9-13); etching a set of apertures **5** through said

pad insulator and said device layer to an isolation depth (figure 2D; col. 4, lines 20-24); depositing an isolation insulator layer 7 in said apertures to a depth sufficient to fill said apertures above said device layer by a first margin and having a sidewall thickness on aperture walls (figure 2E; col. 4, lines 25-41); etching said isolation insulator layer such that said sidewall thickness of said isolation insulator on said aperture walls is removed and remaining isolation plugs of said isolation insulator layer fill said apertures with an isolation plug surface above said device layer surface by a second margin (figure 2F; col. 4, lines 42-62); and etching said pad insulator layer with an etchant that does not attack said isolation insulator layer, whereby said pad insulator is removed and said isolation plugs fill said apertures without CMP (figure 2J; col. 5, lines 9-13). In addition, Sato shows, pertaining to claim 15, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount (figure 2F; col. 4, lines 42-61). Also, Sato shows, pertaining to claim 16, in which said first margin is greater than said sidewall threshold amount (figure 2F; col. 4, lines 42-61). Sato shows, pertaining to claim 17, in which said pad thickness is such that said sidewall thickness is less than a sidewall threshold amount (figure 2F; col. 4, lines 42-61). In addition, Sato shows, pertaining to claim 18, in which said first margin is greater than said sidewall threshold amount (figure 2F; col. 4, lines 42-61). Finally, Sato shows, pertaining to claim 20, in which said field apertures are formed only in areas of pad nitride disposed between apertures separated by greater than a minimum active area distance (figure 2D; col. 4, lines 20-24).

However, Sato fails to show, pertaining to claim 10, implanting said pad insulator with ions such that implanted areas of said pad insulator with ions such that implanted areas of said pad insulator have an etch rate substantially greater than unimplanted areas of said pad insulator.

In addition, Sato fails to show, pertaining to claim 11, in which at least areas of pad nitride disposed between apertures separated by greater than a minimum active area distance are implanted. Also, Sato fails to show, pertaining claim 12, in which only areas of pad nitride disposed between apertures separated by greater than a minimum active are distance are implanted. Sato fails to show, pertaining to claim 13, in which said ions have implantation energy such that less than a threshold amount of ions penetrate said device layer. Finally, Sato fails to show, pertaining to claim 14, in which said ions have an implantation energy such that at least a threshold concentration of ions extend throughout said pad insulator layer.

Chung teaches, on figure 2F, and corresponding text, a similar shallow trench isolation method that includes an ion implantation step within the pad nitride film (col. 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art to substitute the following steps: implanting said pad insulator with ions such that implanted areas of said pad insulator with ions such that implanted areas of said pad insulator have an etch rate substantially greater than unimplanted areas of said pad insulator; in which at least areas of pad nitride disposed between apertures separated by greater than a minimum active area distance are implanted; in which only areas of pad nitride disposed between apertures separated by greater than a minimum active are distance are implanted; in which said ions have an implantation energy such that less than a threshold amount of ions penetrate said device layer; in which said ions have an implantation energy such that at least a threshold concentration of ions extend throughout said pad insulator layer, in the method of Sato, pertaining to claims 10-14, according to the teachings of Chung, with the motivation that, by using the pad nitride film (pad insulator) as a mask, the substrate would be protected from the implantation step. In addition, having an implantation step, may

also improve formation of the field recess at the upper edges of the isolation region, allowing a more efficient removal of insulation films, during an etching process.

Allowable Subject Matter

Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record, Sato et al., US Patent 6,798,038 alone or in view of Chung US Patent 6,653,201, fails to show, pertaining to claim 21, "...performing before said step of forming set of apertures in areas of pad insulator...".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
June 9, 2005

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